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(54) Frequency division multiplexed transmission of synchronous and start-stop data

Frequenzmultiplexübertragung von synchronen Daten und Start-Stop-Daten

Transmission à multiplexage fréquentiel de données synchrones et de données marche-arrêt

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- **NEC RESEARCH AND DEVELOPMENT no. 92 , January 1989 , TOKYO JP pages 33 - 37 XP98392 K. DOI ET AL.: 'A Digital Signal Processor for Modem Application.'**

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Description

(1) Field of the Invention

The present invention relates to a modulator, a demodulator, and a modem containing the modulator and the demodulator. The present invention is applicable, in particular, to a modem having provision for modulating and demodulating signals carrying information on conditions of the modem and another modem connected with the modem through an analog transmission line, through a secondary channel which is provided in addition to a main channel. The main channel and the secondary channel are frequency division multiplexed within a frequency band of the analog transmission line.

Figure 1 is a diagram illustrating an on-line information processing system wherein a plurality of pieces of data terminal equipment are connected through analog transmission lines to a host computer. In Fig. 1, reference numeral 900 denotes a host computer, 901 denotes a communication control processor, 903 denotes a network monitoring apparatus, 911_1 to 911_n each denote a modem on the host computer side, 912_1 to 912_n each denote a modem on the terminal side, 913_1 to 913_n each denote a piece of data terminal equipment, and 914_1 to 914_n each denote an analog transmission line. For example, the host computer 900 and the communication control processor 901 are provided in a main office of a company, and the plurality of pieces of data terminal equipment are respectively positioned in a plurality of branch offices. Digital signals are transmitted between the host computer 900 and the plurality of pieces of data terminal equipment 913_1 to 913_n through the analog transmission lines 914_1 to 914_n. When transmitting the digital signals through the analog transmission lines 914_1 to 914_n, the digital signals are modulated to analog signals by the modulators on transmitter sides, transmitted through the analog transmission lines, and demodulated to digital signals by the demodulators on receiver sides. Each modem 911_1 to 911_n and 914_1 to 914_n has provision for monitoring various conditions thereof, and a secondary channel is provided in addition to a main channel for transmitting the above digital signals.

As mentioned above, the main channel and the secondary channel are frequency division multiplexed within a frequency band of the analog transmission line. Figure 2 is a diagram illustrating frequency bands allocated for the main channel and the secondary channel within the frequency band of the analog transmission line (0.3 to 3.4 kHz). As indicated in Fig. 2, the frequency band for the secondary channel is allocated on the lower frequency side of the frequency band of the main channel, separated from the frequency band of the main channel. In the example of Fig. 2, the frequency band of the main channel ranges from 600 to 3,000 Hz, and the frequency band of the secondary channel ranges from 311 to 359 Hz. The center frequencies of the frequency bands of the main channel and the secondary channel are 1,800 and 335 Hz, respectively.

The network monitoring apparatus 903 collects information on the conditions monitored by the respective modems 911_1 to 911_n and 914_1 to 914_n through the above secondary channels and the signal lines 915_1 to 915_n. Figure 3 is a diagram illustrating a connection between the network monitoring apparatus 903 and the plurality of modems 911_1 to 911_n on the side of the host computer 900. As indicated in Fig. 3, the plurality of modems 911_1 to 911_n are connected with the network monitoring apparatus 903 in the form of a bus connection. The signal lines 915_1 to 915_n connecting the network monitoring apparatus 903 with the plurality of modems 911_1 to 911a are balanced signal lines in accordance with RS485, and the network monitoring apparatus 903 collects the above information by polling the respective modems 915_1 to 915_n. In the communication between the network monitoring apparatus 903 and the plurality of modems 911_1 to 911_n, a start-stop system is used, i. e., a start bit and a stop bit are affixed to each character (comprised of eight bits) in the information transmitted between the network monitoring apparatus 903 and the plurality of modems 911_1 to 911a.

Figure 4 is a diagram illustrating a construction of a conventional modem which can be used in the system as indicated in Fig. 1. In Fig. 4, reference numeral 800 denotes a piece of data terminal equipment, 110a to 110i each denote a driver circuit, 40' denotes a main signal modulation unit, 50' denotes a main signal demodulation unit, 60a denotes a secondary signal modulation unit, 60b denotes a secondary signal demodulation unit, 70' denotes a microprocessor unit (MPU) as a command control unit, 41' and 51' each denote a microprocessor unit, 42' and 52' each denote a digital signal processor (DSP), 43' and 53' each denote a digital to analog converter, 11 denotes a signal adder, 90a and 90b each denote a low-pass filter, 90c and 90d each denote a high-pass filter, and 903 denotes the network monitoring apparatus of Fig. 1.

In the construction of Fig. 4, digital signals supplied from the data terminal equipment 800 are modulated to analog passband signals within the frequency band of the main channel in the main signal modulation unit 40' to be supplied to the signal adder 11. A command or data to be transmitted through the analog transmission line is generated by the microprocessor unit 70', modulated to an analog passband signal in the secondary signal modulation unit 60a, and filtered through the low-pass filter 90a to be supplied to the signal adder 11. Analog signals transmitted from the analog transmission line are supplied to the main signal demodulation unit 50' and the low-pass filter 90b. Frequency components corresponding to the main channel in the analog signals pass through the high-pass filter 90d, are converted to digital signals, and demodulated through the digital signal processor 52' and the microprocessor unit 51'. Frequency components corresponding to the secondary channel in the analog signals pass through the low-pass

filter 90b, are converted to digital signals, and demodulated through the secondary signal demodulation unit 60b. The demodulated secondary signals are supplied to the microprocessor unit 70'.

Conventionally, the modulation and demodulation of the main signals are performed in accordance with phase shift keying (PSK) or quadrature amplitude modulation (QAM), and the modulation and demodulation of the secondary signals are performed in accordance with frequency shift keying (FSK). The demodulation in accordance with the frequency shift keying (FSK) can be performed without synchronization with a receiving clock signal regenerated from the received signal, while the demodulation in accordance with the phase shift keying (PSK) or the quadrature amplitude modulation (QAM) must be performed in synchronization with the receiving clock. Therefore, the modulation and demodulation of the main signals are performed by using the digital signal processor and the microprocessor unit, and the modulation and demodulation of the secondary signals are performed by using a one chip modem, which is commercially available and realizes the secondary signal modulation unit 60a and the secondary signal demodulation unit 60b.

Since the modulation and demodulation of the main signals and the secondary signals are carried out in separate hardware, the amount of the hardware is increased, and therefore, the size of and the cost of the modem are increased.

An arrangement of a generally similar type to that explained above is disclosed in FR-A-2 620 583, which also discloses the features of the preamble of each independent claim.

According to the first aspect of the present invention, there is provided a modulator comprising: a first modulating means for receiving a first digital signal, and modulating the first digital signal to generate a first modulated signal, where frequency components contained in the first modulated signal are within a first frequency band; a second modulating means for receiving another digital signal, and modulating it to generate a second modulated signal, where frequency components contained in the second modulated signal are within a second frequency band which is separated from the first frequency band; and a signal adding means for receiving the first and second modulated signals, and adding the first and second modulated signals to generate a frequency division multiplexed signal; characterised by a transforming means for receiving a second digital signal containing at least one set of a predetermined number of successive bits corresponding to a character data, a start bit preceding each set of the predetermined number of successive bits, and a stop bit following each set of the predetermined number of successive bits, and removing the start bit and the stop bit from the second digital signal to generate a third digital signal containing the character data as said another digital signal received by said second modulating means.

According to the second aspect of the present invention, there is provided a demodulator comprising: a first demodulating means for receiving a frequency division multiplexed signal and for regenerating a first digital signal, wherein first and second modulated signals are frequency division multiplexed in the frequency division multiplexed signal and wherein frequency components contained in the first modulated signal are within a first frequency band and frequency components contained in the second modulated signal are within a second frequency band which is separated from the first frequency band, the first modulated signal being equivalent to a signal generated by modulating the first digital signal, and the second modulated signal being equivalent to a signal generated by modulating a second digital signal; and a second demodulating means for receiving the frequency division multiplexed signal and regenerating the second digital signal containing at least one set of a predetermined number of successive bits corresponding to a character data; characterised by a transforming means for receiving the second digital signal and inserting a start bit before each set of the predetermined number of successive bits and a stop bit after each set of the predetermined number of successive bits to generate a third digital signal in a start-stop system.

Embodiments of the present invention may provide a modulator, a demodulator, or a modem containing provision for modulating and demodulating a secondary signal which is frequency division multiplexed with a main signal, where the size thereof and the cost for manufacturing the modulator, the demodulator, or the modem is reduced.

Embodiments of the present invention may also provide a modulator, a demodulator, or a modem containing provision for modulating and demodulating a secondary signal which is frequency division multiplexed with a main signal, where efficiency in transmission of the secondary signal is increased.

For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, wherein:

Figure 1 is a diagram illustrating an on-line information processing system wherein a plurality of pieces of data terminal equipment are connected through analog transmission lines to a host computer;

Figure 2 is a diagram illustrating frequency bands allocated for the main channel and the secondary channel within the frequency band of the analog transmission line (0.3 to 3.4 kHz);

Figure 3 is a diagram illustrating a connection between the network monitoring apparatus 903 and the plurality of modems 911_1 to 911_n;

Figure 4 is a diagram illustrating a construction of a conventional modem which can be used in the system as indicated in Fig. 1;

Figure 5 is a diagram illustrating a basic construction of the modem according to an embodiment of the invention;
Figure 6 is a diagram illustrating the hardware construction of the modem as an embodiment of the present invention;
Figures 7, 8 and 9 are a block diagram illustrating the construction of the modem as an embodiment of the present invention;
Figure 10 is a diagram illustrating a bit series and each predetermined number of successive bits corresponding to each symbol;
Figure 11 is a diagram illustrating a bit series containing a character data accompanied with a start bit and a stop bit; and
Figure 12 is a diagram illustrating character data stored in the data storage unit.

Figure 5 is a diagram illustrating a basic construction of the modem according to an embodiment of the present invention. In Fig. 5, reference numeral 1 denotes a main signal modem unit, 3 denotes a signal transformation unit, 4 denotes a signal adder, 5 denotes a signal processing portion, 6 denotes a secondary signal modem unit, and 7 denotes a command control unit. The main signal modem unit 1 and the secondary signal modem unit 6 each contain a modulator and a demodulator. Preferably, the main signal modem unit 1, the signal transformation unit 3, the signal adder 4, and the secondary signal modem unit 6 are realized by at least one digital signal processor. Namely, the main signal modem unit 1, the data transformation unit 3, the signal adder 4, and the secondary signal modem unit 6 are realized by software.

First, the modulating operations carried out in the construction of Fig. 5 are explained below. In the construction of Fig. 5, a first digital signal (main signal) is supplied to the main signal modem unit 1, and the main signal modem unit 1 modulates the first digital signal to generate and supply to the signal adder 4 a first modulated signal (corresponding to a first analog signal). Frequency components contained in the first modulated signal are within a first frequency band. The first digital signal may be a digital signal synchronized with a clock (timing) signal, and the modulation in the main signal modem unit 1 is carried out synchronized with a clock signal. The clock signal used in the modulation may be one of the following clock signals:

(1) a clock signal generated within the modulator (the clock signal generated within a modem is known as the ST2 signal, which is supplied to a piece of data terminal equipment supplying the main signal to the modem synchronized with the ST2 signal);
(2) a clock signal supplied from outside (typically from a piece of data terminal equipment supplying the main signal to the modem) of the modulator (the clock signal supplied from a piece of data terminal equipment together with the main signal is known as the ST1 signal, the data terminal equipment supplies the main signal synchronized with the ST1 signal);
(3) a clock signal regenerated from the received digital signal (main signal), which is known in the conventional modem as the RT signal;
(4) a clock signal regenerated from an analog signal in the main channel received in a demodulator accompanied by the modulator; and
(5) a clock signal regenerated from an analog signal in the secondary channel received in the demodulator, the demodulator being accompanied by the modulator.

Parallel to the above operation, a second digital signal is supplied to the signal transformation unit 3. The second digital signal contains at least one set of a predetermined number of successive bits corresponding to a character, a start bit preceding each set of the predetermined number of successive bits, and a stop bit following each set of the predetermined number of successive bits. The second digital signal may be generated by the command control unit 7. The signal transformation unit 3 receives the second digital signal, and removes the start bit and the stop bit from the second digital signal to generate and supply to the secondary signal modem unit 6 a third digital signal. Frequency components contained in the second modulated signal are within a second frequency band which is separated from the first frequency band. The secondary signal modem unit 6 receives the third digital signal, and modulates the third digital signal to generate and supply to the signal adder 4 a second modulated signal (corresponding to a second analog signal). The third digital signal may be a digital signal synchronized with a clock signal, and the modulation in the secondary signal modem unit 6 may be carried out synchronized with a clock signal. The clock signal used in the modulation may be the same (common) clock signal as used in the main signal modem unit 1. The signal adder 4 adds the above first and second modulated signals (first and second analog signals) to generate a frequency division multiplexed signal.

Preferably, the main signal modem unit 1 and the secondary signal modem unit 6 may perform the same type of modulation. Thereby, portions of hardware and software can be made common to the modulating operations in both the main signal modem unit 1 and the secondary signal modem unit 6. Namely, the size of the hardware and software and cost for realizing the main signal modem unit 1 and the secondary signal modem unit 6 can be made small. Since, conventionally the main signal is modulated by the phase shift keying (PSK) or the quadrature amplitude modulation (QAM), and the modulating operation for the phase shift keying (PSK) or the quadrature amplitude modulation (QAM) is

performed in synchronization with a clock signal. Therefore, the modulating operation in the secondary signal modem unit 6 must be performed in synchronization with a clock signal when the phase shift keying (PSK) or the quadrature amplitude modulation (QAM) is used. In this case, the third digital signal supplied from the signal transformation unit 3 to the secondary signal modem unit 6 must be synchronized with a clock signal. Namely, in this case, the signal transformation unit 3 transforms the second digital signal in the start-stop system to the third digital signal in the clock-synchronization system.

Alternatively, considering the high transmission rate in the main channel and the low transmission rate in the secondary channel, the quadrature amplitude modulation (QAM) may be used for the modulation in the main channel, and the phase shift keying (PSK) may be used for the modulation in the secondary channel. In this case, portions of hardware and software can also be made common to the modulating operations in both the main signal modem unit 1 (by the quadrature amplitude modulation (QAM)) and the secondary signal modem unit 6 (by the phase shift keying (PSK)). Namely, the size of the hardware and software and cost for realizing the constructions for the modulation in the main signal modem unit 1 and the secondary signal modem unit 6 can be made small. The reason for the above is that the quadrature amplitude modulation (QAM) contains common or similar operations to the operations in the phase shift keying (PSK).

Secondly, the demodulating operations carried out in the construction of Fig. 5 are explained below. In the construction of Fig. 5, a frequency division multiplexed modulated signal is supplied to the main signal modem unit 1 and the secondary signal modem unit 6. The frequency division multiplexed modulated signal is a signal wherein first and second modulated signals are frequency division multiplexed, frequency components contained in the first modulated signal are within the above first frequency band, and frequency components contained in the second modulated signal are within the above second frequency band which is separated from the first frequency band. In the main signal modem unit 1, a first base band signal which is equivalent to a signal generated by demodulating the first modulated signal, is obtained. The first base band signal is a digital signal synchronized with a clock signal regenerated from the first base band signal. Parallel to the above demodulating operation in the main signal modem unit 1, in the secondary signal modem unit 6, a second base band signal which is equivalent to a signal generated by demodulating the second modulated signal, is obtained. The second base band signal is a digital signal synchronized with a clock signal regenerated from the second base band signal, and contains at least one set of a predetermined number of successive bits corresponding to a character. The second base band signal is supplied to the signal transformation unit 3. In the signal transformation unit 3, a start bit is inserted before each set of the predetermined number of successive bits, and a stop bit is inserted after each set of the predetermined number of successive bits to generate a secondary signal in a start-stop system.

Similar to the modulation explained above, the first and second modulated signals are preferably modulated by the same type of modulation, and thus the main signal modem unit 1 and the secondary signal modem unit 6 perform the same type of demodulation. Thereby, portions of hardware and software can be made common to the demodulating operations in both the main signal modem unit 1 and the secondary signal modem unit 6. Namely, the size of the hardware and software and cost for realizing the main signal modem unit 1 and the secondary signal modem unit 6 can be made small. Since, conventionally the main signal is modulated by the phase shift keying (PSK) or the quadrature amplitude modulation (QAM), and the demodulating operation for the phase shift keying (PSK) or the quadrature amplitude modulation (QAM) is performed in synchronization with a clock signal regenerated from the first base band signal. Therefore, the demodulating operation in the secondary signal modem unit 6 must be performed in synchronization with a clock signal when the phase shift keying (PSK) or the quadrature amplitude modulation (QAM) is used. In this case, the second base band signal supplied from the secondary signal modem unit 6 to the signal transformation unit 3 must a synchronized with the clock signal. Namely, in this case, the signal transformation unit 3 transforms the second digital signal in the start-stop system to the second base band signal (secondary signal) in the clock-synchronization system.

Similar to the modulation explained above, alternatively, considering the high transmission rate in the main channel and the low transmission rate in the secondary channel, the quadrature amplitude modulation (QAM) may be used in the main channel, and the phase shift keying (PSK) may be used in the secondary channel. In this case, portions of hardware and software can also be made common to the demodulating operations in both the main signal modem unit 1 (by the quadrature amplitude modulation (QAM)) and the secondary signal modem unit 6 (by the phase shift keying (PSK)). Namely, the size of the hardware and software and cost for realizing the constructions for the demodulation in the main signal modem unit 1 and the secondary signal modem unit 6 can be made small.

Figure 6 is a diagram illustrating the hardware construction of the modem as an embodiment of the present invention. In Fig. 6, reference numeral 40 denotes a modulation unit, 50 denotes a demodulation unit, 41 and 51 each denote a microprocessor unit, 42 and 52 each denote a digital signal processor (DSP), 43 and 53 each denote a digital to analog converter, 70 denotes a microprocessor unit (MPU) as a command control unit, 80 denotes a DTE interface circuit, 81 denotes a MDMS (modem monitoring system) interface circuit, 91 and 98

each denote a low-pass filter, 92 and 95 each denote an amplifier, and 93 and 94 each denote a transformer. The DTE interface circuit 80 is provided for shifting levels of the signals between the modem and the data terminal equipment. In the DTE interface circuit 80, RS denotes a terminal for a signal of "Request to Send", CS denotes a terminal for a signal of "Clear to Send", SD denotes a terminal for a signal of "Transmitted Data", CD denotes a terminal for a signal of "Clear Detector", RD denotes a terminal for a signal of "Received Data", ST2 denotes a terminal for a timing signal of "Send Timing", and RT denotes a terminal for a timing signal of "Receive Timing". Namely, timing signals ST2 and RT are transmitted between the modem and the data terminal equipment 800 in synchronization with the data signals SD and RD, respectively.

In the construction of Fig. 6, a main digital signal supplied from the data terminal equipment is supplied through the DTE interface circuit 80 to the modulation unit 40, and modulated to a first passband signal within the frequency band of the main channel by the microprocessor unit 41 and the digital signal processor 42 in the modulation unit 40. A digital signal carrying a command or data to be transmitted through the analog transmission line is generated by the microprocessor unit 70, and is also supplied to the modulation unit 40 to be modulated to a second passband signal within the frequency band of the secondary channel by the microprocessor unit 41 and the digital signal processor 42 in the modulation unit 40. The first and second passband signals are summed, and the summed passband signal is converted to an analog passband signal. The analog passband signal generated in the modulation unit 40 is filtered through the low-pass filter to eliminate unnecessary frequency components, amplified in the amplifier 92, and transmitted through the transformer 93 and the terminal S onto the analog transmission line.

An analog passband signal transmitted through the analog transmission line is received at the terminal R, and transformed by the transformer 94, amplified in the amplifier 93, and filtered through the low-pass filter 98 to be supplied to the demodulation unit 50. In the demodulation unit 50, the analog passband signal output from the low-pass filter 98 is converted to a digital passband signal by the analog to digital converter 53. The digital passband signal is demodulated to generate first and second base band signals by the microprocessor unit 51 and the digital signal processor 52, where frequency components of the first base band signal are within the frequency band of the main channel, and frequency components of the second base band signal are within the frequency band of the secondary channel. The first base band signal is supplied to the DTE interface circuit 80, and the second base band signal is supplied to the microprocessor unit 70.

The network monitoring apparatus 903 (Fig. 1) sends a first command to the microprocessor unit 70 in each of the modems at the near end (such as the modems 911_1 to 911_n in Fig. 1) directly connected to the network monitoring apparatus 903 through the MDMS interface circuit 81 in the modem. The first command requests information on the conditions of the modems at the near end, and the modems at the far end (such as the modems 912_1 to 912_n in Fig. 1) connected to the modems at the near end through the analog transmission lines. When the command requests the information on the conditions of the modem at the near end, the modem at the near end returns the information on the conditions of the modem to the network monitoring apparatus 903 through the MDMS interface circuit 81. When the command requests the information on the conditions of the modem at the far end, the modem at the near end generates a secondary signal carrying a second command requesting the information on the conditions of the modem at the far end, which is connected to the modem at the near end through the analog transmission line, and supply the secondary signal to the modulation unit 40 to be modulated and transmitted to the modem at the far end through the secondary channel. When the modem at the far end receives the modulated secondary signal through the secondary channel, the modulated secondary signal is demodulated to regenerate a secondary signal, and the secondary signal is supplied to the microprocessor unit 70 in the modem at the far end. In response to the second command, the modem at the far end generates and returns a first response containing the requested information through the secondary channel to the microprocessor unit 70 in the modem at the near end. Receiving the first response, the microprocessor unit 70 in the modem at the near end generates and returns a second response containing the requested information through the MDMS interface circuit 81 to the network monitoring apparatus 903. The MDMS interface circuit 81 is provided for converting an unbalanced signal carrying the above response and transmitted from the microprocessor unit 70, to a balanced signal, and converting a balanced signal carrying the above command and transmitted from the network monitoring apparatus 903, to an unbalanced signal.

Figures 7, 8 and 9 are a block diagram illustrating the construction of the modem as an embodiment of the present invention. Details of the DTE interface circuit 80 and the modulation unit 40 are indicated in Fig. 7, details of the analog to digital converter 53 and the demodulation unit 52 in the demodulation unit 50 are indicated in Fig. 8, and details of the microprocessor unit 51 in the demodulation unit 50 are indicated in Fig. 9.

In Fig. 7, reference numerals 11a and 11b each denote a scrambler unit, 12a and 12b each denote a code transformation unit, 13a and 13b each denote a roll-off filter, 14a and 14b each denote a modulator unit, 16 denotes an equalizer, 17 denotes an attenuator, 18a and 18b each denote a pattern generating unit, 31 denotes a start & stop bit removing unit, 32 denotes a data storage unit, 33 denotes a start & stop bit inserting unit, and 44 denotes a common memory. The operations of the

modulation unit 40 are controlled by the microprocessor unit 41, and the digital signal processor 42 operates under the control of the microprocessor unit 41. The elements indicated by a block in the microprocessor unit 41 and the digital signal processor 42 may be respectively realized by a software unit, and the operations of the respective software units are performed by a multitask operation under the control of the microprocessor unit 41, although any unit may be replaced by a hardware unit performing the same operation. The digital signal processor 42 may comprise more than one digital signal processor. In this case, a multi-processor system is constructed by the more than one digital signal processor and the microprocessor unit 41, and the microprocessor unit 41 controls the multi-processor system. The common memory 44 is provided for common use by the microprocessor unit 41 and the digital signal processor 42. The microprocessor unit 41 and the (or each) digital signal processor 42 can access the common memory 44 in a time sharing manner. A command from the microprocessor unit 41 is given to the digital signal processor 42 when the command is written in a predetermined address in the common memory 44 by the microprocessor unit 41 and read by the digital signal processor 42.

The pattern generating units 18a and 18b are provided for generating predetermined patterns to be inserted in training signals which are transmitted preceding the main signal and the secondary signal, respectively. The patterns generated by the pattern generating units 18a and 18b may be supplied to the inputs of the scrambler units 11a and 11b, respectively, or to the inputs of the code transformation units 12a and 12b, respectively.

The main signal supplied to the modulation unit 40 from the data terminal equipment through the DTE interface circuit 80, is scrambled by the scrambler unit 11a, and each predetermined number of successive bits (corresponding to each symbol) in the scrambled main signal (as indicated in Fig. 10) is transformed to a data signal point in a vector signal space in accordance with a predetermined coding method, for example, as stipulated in the CCITT recommendation V.27 for the phase shift keying modulation, or in the CCITT recommendation V.29 for the quadrature amplitude modulation. The output of the code transformation unit 12a is supplied to the roll-off filter 13a provided in the digital signal processor 42 to eliminate components other than the base band components in the output of the code transformation unit 12a. The output of the roll-off filter 13a is supplied to the modulator unit 14a to be modulated to generate a first passband signal where frequency components contained in the first passband signal are within the first frequency band corresponding to the main channel.

Parallel to the above modulating operation of the main signal, the secondary signal supplied from the microprocessor unit 70 is supplied to the start & stop bit removing unit 31 in the microprocessor unit 41. The secondary signal supplied from the microprocessor unit 70 to the modulation unit 40 contains at least one set of a predetermined number of (for example, eight) successive bits representing to a character data, a start bit preceding each set of the predetermined number of successive bits, and a stop bit following each set of the predetermined number of successive bits, as indicated in Fig. 11. The start & stop bit removing unit 31 removes the start bit and the stop bit in a bit series carried by the secondary signal, and the character data represented by the set of the predetermined number of successive bits is temporarily stored in the data storage unit 32, as indicated in Fig. 12. The data storage unit 32 is necessary when the transmission rate in the transmission of the secondary signal between the microprocessor unit 70 and the modulation unit 40 is higher compared with the transmission rate in the secondary channel through the analog transmission line. In this embodiment, the transmission rate in the transmission of the secondary signal between the microprocessor unit 70 and the modulation unit 40 may be 8 kbps, and the transmission rate in the secondary channel through the analog transmission line may be 75 bps. Thus, the operation of the microprocessor unit 70 is not affected by the low transmission rate in the secondary channel.

The microprocessor unit 41 monitors the data storage unit 32 regarding whether or not any character data is stored therein. When the microprocessor unit 41 determines that any character data is stored in the data storage unit 32, the microprocessor unit 41 activates the modulator unit 14b in the digital signal processor 42 and the pattern generation unit 18b to generate a carrier signal for the secondary channel and transmit a training signal for the secondary channel . The carrier signal for the secondary channel is generated in the modulator unit 14b. Then, the microprocessor unit 41 reads out each character data stored in the data storage unit 32 in the order each character data is stored therein to supply the character data to the start & stop bit inserting unit 33. When the microprocessor unit 41 determines that no character data is remaining in the data storage unit 32, the microprocessor unit 41 controls the digital signal processor 42 to stop the transmission of the carrier signal for the secondary channel. The start & stop bit inserting unit 33 inserts a start bit before each character data, and a stop bit after each character data to generate a bit series as indicated in Fig. 11. The start bit and the stop bit are inserted so that each character data can easily be recognized when the bit series is received and demodulated in the modem at the other end of the analog transmission line. The bit series generated by the start & stop bit inserting unit 33 is supplied to the scrambler 11b to scramble the bit series, and the scrambled bit series is supplied to the code transformation unit 12b. Each predetermined number of successive bits (corresponding to each symbol) in the scrambled main signal (as indicated in Fig. 10) is transformed to a data signal

point in a vector signal space in accordance with a predetermined coding method, for example, as stipulated in the CCITT recommendation V.27 for the phase shift keying modulation, or in the CCITT recommendation V. 29 for the quadrature amplitude modulation. As explained before, preferably, the same type of modulation as in the main channel is used in the secondary channel. The output of the code transformation unit 12b is supplied to the roll-off filter 13b provided in the digital signal processor 42 to eliminate components other than the base band components in the output of the code transformation unit 12b. The output of the roll-off filter 13b is supplied to the modulator unit 14b to be modulated to generate a second passband signal where frequency components contained in the second passband signal are within the second frequency band corresponding to the secondary channel.

The outputs of the modulator units 14a and 14b are summed by the signal adder 15 to generate a frequency division multiplexed passband signal. The frequency division multiplexed passband signal is then equalized by the equalizer unit 16, attenuated by the attenuator 17, and converted to an analog form by the digital to analog converter 43.

As explained above, a pair of software units performing similar operations are provided for the respective operations such as the scrambling operation, the code transformation, the roll-off filtering, and the modulation. Therefore, software and hardware in the microprocessor unit 41 and the digital signal processor 42 can be made common, and thus the total size of and cost for the software and hardware can be reduced.

In Fig. 8, reference numerals 20a and 20b each denote a demodulator unit, 21a and 21b each denote a timing regeneration unit, 22a and 22b each denote a band separation unit, 23a and 23b each denote an automatic gain control unit, 24a and 24b each denote an automatic equalizer unit, 25a and 25b each denote a carrier detection unit, 28 denotes a condition monitor unit, and 54 denotes a common memory. The elements indicated by a block in the microprocessor unit 51 and the digital signal processor 52 may be respectively realized by a software unit, and the operations of the respective software units are performed by a multi-task operation under the control of the microprocessor unit 51, although any unit may be replaced by a hardware unit performing the same operation. The digital signal processor 52 may comprise more than one digital signal processor. In this case, a multi-processor system is constructed by the more than one digital signal processor and the microprocessor unit 51, and the microprocessor unit 51 controls the multi-processor system.

The analog frequency division multiplexed passband signal filtered through the low-pass filter 98 in Fig. 6 is supplied to the analog to digital converter 53 to be converted to a digital form. Then, the frequency division multiplexed passband signal is supplied to the demodulator units 20a and 20b.

The demodulator unit 20a receives the frequency division multiplexed passband signal, and shifting frequencies of the frequency division multiplexed passband signal by a first predetermined frequency (-1,800 Hz corresponding to the center frequency of the frequency band for the main channel as indicated in Fig. 2) to transform the frequency division multiplexed passband signal to a first base band signal. Then, the output of the demodulator 20a is supplied to the band separation filter 22a to eliminate frequency components other than the frequency components within the frequency band for the main channel, and thus a first base band signal is obtained as an output of the band separation filter 22a. The amplitude of the output of the band separation filter 22a is controlled by the automatic gain control unit 23a, and the output of the automatic gain control unit 23a is equalized by the automatic equalizer unit 24a. The output of the automatic equalizer unit 24a is supplied to the code transformation unit 26a in the microprocessor unit 51 indicated in Fig. 9. The timing information in the received signal in the secondary channel is extracted from the output of the demodulator unit 20a by the timing regeneration unit 21a, and the carrier detection is carried out by the carrier detection unit 25a by monitoring the output of the band separation filter unit 22a. Further, to obtain the information on the conditions of the modem, the condition monitor unit 28 is provided. The condition monitor unit 28 monitors the received and demodulated signal to examine the signal to noise ratio (S/N) in the received signal, and an error rate in the demodulated signal, and the condition monitor unit 28 also monitors alarm conditions of the modem. The information on the conditions of the modem, obtained by the condition monitor unit 28, is written in predetermined addresses in the common memory 54.

The common memory 54 is provided for common use by the microprocessor unit 51 and the digital signal processor 52. The microprocessor unit 51 and the (or each) digital signal processor 52 can access the common memory 54 in a time sharing manner. A command from the microprocessor unit 51 is given to the digital signal processor 52 when the command is written in a predetermined address in the common memory 54 by the microprocessor unit 51 and read by the digital signal processor 52.

Parallel to the above demodulating operation in the main channel, the demodulator unit 20b receives the frequency division multiplexed passband signal, and shifting frequencies of the frequency division multiplexed passband signal by a second predetermined frequency (-335 Hz corresponding to the center frequency of the frequency band for the secondary channel as indicated in Fig. 2) to transform the frequency division multiplexed passband signal to a second base band signal. Then, the output of the demodulator 20b is supplied to the band separation filter 22b to eliminate frequency components other than the frequency components within the frequency band for the secondary channel, and thus a

second base band signal is obtained as an output of the band separation filter 22b. The amplitude of the output of the band separation filter 22b is controlled by the automatic gain control unit 23b, and the output of the automatic gain control unit 23b is equalized by the automatic equalizer unit 24b. The output of the automatic equalizer unit 24b is supplied to the code transformation unit 26b in the microprocessor unit 51 indicated in Fig. 9. The timing information in the received signal in the secondary channel is extracted from the output of the demodulator unit 20b by the timing regeneration unit 21b, and the carrier detection is carried out by the carrier detection unit 25b by monitoring the output of the band separation filter unit 22b.

In Fig. 9, reference numerals 26a and 26b each denote a code transformation unit, 27a and 27b each denote a descrambler unit, 34 denotes a start & stop bit inserting unit, 35 denotes a data storage unit, and 36 denotes a start & stop bit removing unit.

The output of the automatic equalizer unit 24a represents a data signal point in the vector signal space for each symbol corresponding to the predetermined number of successive bits carried by the main signal. The code transformation unit 26a receives the output of the automatic equalizer unit 24a, and transforms each data signal point to the corresponding predetermined number of successive bits to obtain a scrambled bit series. The scrambled bit series is descrambled by the descrambler unit 27a to regenerate a descrambled bit series transmitted through the main channel.

Parallel to the above operation in the main channel, the output of the automatic equalizer unit 24b represents a data signal point in the vector signal space for each symbol corresponding to the predetermined number of successive bits carried by the secondary signal. The code transformation unit 26b receives the output of the automatic equalizer unit 24b, and transforms each data signal point to the corresponding predetermined number of successive bits to obtain a scrambled bit series. The scrambled bit series is descrambled by the descrambler unit 27b to regenerate a descrambled bit series transmitted through the secondary channel. Due to the provision of the start 8 stop bit inserting unit 33 in the microprocessor unit 41 in Fig. 7, the descrambled bit series in the secondary channel contains the start bit and the stop bit before and after each character data as indicated in Fig. 11. The start & stop bit removing unit 36 receives the descrambled bit series output from the descrambler unit 27b, and removes the start bit and the stop bit before and after each character data. Each character data is temporarily stored in the data storage unit 35 as indicated in Fig. 12. As explained above, the operations from the receipt of the secondary signal to the temporary storage in the data storage 35 are carried out with a low rate corresponding to the low transmission rate in the secondary channel. Then, each character data stored in the data storage unit 35 is read out in the order each character data is stored therein, and a start bit and a stop bit are inserted before and after each character data, respectively, to generate and transmit to the microprocessor unit 70 a bit series in the start & stop system at the high transmission rate.

Besides the above processing operations of the received signals, when requested by the microprocessor unit 70, the microprocessor unit 51 reads the information on the conditions of the modem from the common memory 54, and transmits the same to the microprocessor unit 70. In the transmission of the information, a start bit and a stop bit are inserted before and after each character data of the information by using the start & stop bit inserting unit 33.

As explained above, a pair of software units performing similar operations are provided for the respective operations such as the demodulation, the band separation filtering, the automatic gain control, the automatic equalization, the code transformation, and the descrambling operation. Therefore, software and hardware in the microprocessor unit 51 and the digital signal processor 52 can be made common, and thus the total size of and cost for the software and hardware can be reduced.

Claims

1. A modulator comprising:

a first modulating means (1, 14a) for receiving a first digital signal, and modulating the first digital signal to generate a first modulated signal, where frequency components contained in the first modulated signal are within a first frequency band;

a second modulating means (6, 14b) for receiving another digital signal, and modulating it to generate a second modulated signal, where frequency components contained in the second modulated signal are within a second frequency band which is separated from the first frequency band; and

a signal adding means (4, 15) for receiving the first and second modulated signals, and adding the first and second modulated signals to generate a frequency division multiplexed signal; characterised by

a transforming means (3, 31) for receiving a second digital signal containing at least one set of a predetermined number of successive bits corresponding to a character data, a start bit preceding each set of the predetermined number of successive bits, and a stop bit following each set of the predetermined number of successive bits, and removing the start bit and the stop bit from the second digital signal to generate a third digital signal containing the character data as said another digital signal re-

ceived by said second modulating means (6, 14b).

2. A modulator according to claim 1, further comprising a digital signal generating means (7) for generating the second digital signal to supply the second digital signal to the transforming means (3, 31).

3. A modulator according to claim 1 or claim 2 wherein the first and second modulating means perform the same type of modulation, and the first and second modulating means comprises at least one digital signal processor.

4. A modulator according to claim 3, wherein the first and second modulating means performs one of phase shift keying (PSK) and quadrature amplitude modulation (QAM).

5. A modulator according to claim 1 or 2, wherein at least one portion of the operation performed by the second modulating means is similar to at least one portion of the operation performed by the first modulating means, and the first and second modulating means comprises at least one digital signal processor.

6. A modulator according to claim 5, wherein the first modulating means performs quadrature amplitude modulation (QAM), and the second modulating means performs phase shift keying (PSK).

7. A modulator according to any one of the preceding claims, comprising a data storage means (32), provided between the transforming means (3, 31) and the second modulating means (6, 14b), for temporarily storing the character data contained in the third digital signal, and supplying the character data stored in the data storage means (32) to the second modulating means (6, 14b).

8. A modulator according to claim 7 comprising a start & stop bit inserting means (33), provided between the data storage means (32) and the second modulating means (6, 14b), for receiving each character data from the data storage means (32), inserting a start bit before each character data supplied from the data storage means (32), and a stop bit after each character data, and supplying the character data with the start and stop bits to the second modulating means (6, 14b).

9. A demodulator comprising:

a first demodulating means (1, 20a, 22a) for receiving a frequency division multiplexed signal and for regenerating a first digital signal, wherein first and second modulated signals are frequency division multiplexed in the frequency division multiplexed signal and wherein frequency components contained in the first modulated signal are within a first frequency band and frequency components contained in the second modulated signal are within a second frequency band which is separated from the first frequency band, the first modulated signal being equivalent to a signal generated by modulating the first digital signal, and the second modulated-signal being equivalent to a signal generated by modulating a second digital signal; and
a second demodulating means (6, 20b, 22b) for receiving the frequency division multiplexed signal and regenerating the second digital signal containing at least one set of a predetermined number of successive bits corresponding to a character data; characterised by:
a transforming means (3, 34) for receiving the second digital signal and inserting a start bit before each set of the predetermined number of successive bits and a stop bit after each set of the predetermined number of successive bits to generate a third digital signal in a start-stop system.

10. A demodulator according to claim 9, wherein said first demodulating means (1, 20a, 22a) comprises:

a first frequency shifting means (20a) for receiving the frequency division multiplexed signal and shifting frequencies of the frequency division multiplexed signal by a first predetermined frequency to transform the frequency division multiplexed signal to a fourth digital signal, where the first predetermined frequency corresponds to a center frequency of the first frequency band; and
a first band separation filter means (22a) for receiving the fourth digital signal, and extracting the first digital signal; and wherein
the second demodulating means (6, 20b, 22b) comprises:

a second frequency shifting means (20a) for receiving the frequency division multiplexed signal, and shifting the frequencies of the frequency division multiplexed signal by a second predetermined frequency to transform the frequency division multiplexed signal to a fifth digital signal, where the second predetermined frequency corresponds to a center frequency of the second frequency band; and
a second band separation filter means (22b) for receiving the fifth digital signal, and extracting the second digital signal.

11. A demodulator according to claim 9 or 10, comprising an information decoding means (7) for receiving a digital signal in the start-stop system and decoding information carried by the digital signal.

12. A demodulator according to claim 9, 10 or 11 wherein the first and second modulated signals are modulated by the same type of modulation, and the first and second demodulating means comprises at least one digital signal processor.

13. A demodulator according to claim 12, wherein the first and second modulated signals are modulated by one of phase shift keying (PSK) and quadrature amplitude modulation (QAM).

14. A demodulator according to claim 9, 10 or 11 wherein at least one portion of the operation performed by the second demodulating means is similar to at least one portion of the operation performed by the first demodulating means, and the first and second demodulating means comprises at least one digital signal processor.

15. A demodulator according to claim 14, wherein the demodulating operation performed by the first demodulating means is in accordance with quadrature amplitude modulation (QAM), and the demodulating operation performed by the second demodulating means is in accordance with phase shift keying (PSK).

16. A demodulator according to any one of claims 9 to 15 comprising a data storage means (35), provided between the second demodulating means (6, 20b, 22b) and the transforming means (3, 34), for temporarily storing the character data contained in the second digital signal, and supplying the character data stored in the data storage means (35) to the transforming means (3, 34).

17. A demodulator according to claim 16, wherein the second digital signal further contains a start bit preceding each character data, and a stop bit following each character data, and

said demodulator comprises a start and stop bit removing means (36), provided between the second demodulating means (6, 20b, 22b) and the data storage means (35), for receiving the fourth digital signal from the second demodulating means (6, 20b, 22b), removing a start bit preceding each character data, and a stop bit following each character data, and supplying the character data without the start and stop bits to the data storage means (35).

18. A modem comprising a modulator according to any one of claims 1 to 8 and a demodulator according to any one of claims 9 to 17.

Patentansprüche

1. Modulator, mit:

einer ersten Moduliereinrichtung (1, 14a) zum Empfangen eines ersten digitalen Signals und zum Modulieren des ersten Signals, um ein erstes moduliertes Signal zu erzeugen, wobei die Frequenzkomponenten, die in dem ersten modulierten Signal enthalten sind, innerhalb eines ersten Frequenzbandes liegen;
einer zweiten Moduliereinrichtung (6, 14b) zum Empfangen eines anderen digitalen Signals und zum Modulieren desselben, um ein zweites moduliertes Signal zu erzeugen, wobei die Frequenzkomponenten, die in dem zweiten modulierten Signal enthalten sind, innerhalb eines zweiten Frequenzbandes liegen, welches von dem ersten Frequenzband getrennt ist; und
einer Signaladdiereinrichtung (4, 15) zum Empfangen des ersten und des zweiten modulierten Signals und zum Addieren des ersten und des zweiten modulierten Signals, um ein durch Frequenzteilung gemultiplextes Signal zu erzeugen; **gekennzeichnet** durch
eine Transformiereinrichtung (3, 31) zum Empfangen eines zweiten digitalen Signals, welches wenigstens einen Satz einer vorbestimmten Anzahl von aufeinanderfolgenden Bits enthält, die Zeichendaten entsprechen, wobei ein Startbit jedem Satz der vorbestimmten Zahl von aufeinanderfolgenden Bits vorangeht und wobei ein Stoppbit jedem Satz der vorbestimmten Anzahl von aufeinanderfolgenden Bits nachfolgt, und um das Startbit und das Stoppbit aus dem zweiten digitalen Signal zu entfernen, um ein drittes digitales Signal zu erzeugen, welches die Zeichendaten enthält, und zwar als anderes digitales Signal, welches von der zweiten Moduliereinrichtung (6, 14b) empfangen wird.

2. Modulator nach Anspruch 1, ferner mit einer Digitalsignalgeneratoreinrichtung (7) zum Erzeugen eines zweiten digitalen Signals, um das zweite digitale Signal der Transformiereinrichtung (3, 31) zuzuführen.

3. Modulator nach Anspruch 1 oder Anspruch 2, bei dem die erste und die zweite Modulationseinrichtung den gleichen Modulationstyp ausführen und bei dem die erste und die zweite Modulationseinrichtung wenigstens einen Digitalsignalprozessor aufweisen.

4. Modulator nach Anspruch 3, bei dem die erste und die zweite Modulationseinrichtung eine der folgenden Operationen ausführen: eine Phasenverschiebungsverschlüsselung (PSK) und eine Quadraturamplitudenmodulation (QAM).

5. Modulator nach Anspruch 1 oder 2, bei dem wenigstens ein Abschnitt der Operation, die durch die zweite Modulationseinrichtung ausgeführt wird, ähnlich ist wenigstens einem Abschnitt der Operation, die durch die erste Modulationseinrichtung durchgeführt wird und bei dem die erste und die zweite Modulationseinrichtung wenigstens einen Digitalsignalprozessor enthalten.

6. Modulator nach Anspruch 5, bei dem die erste Modulationseinrichtung eine Quadraturamplitudenmodulation (QAM) durchführt und bei dem die zweite Modulationseinrichtung eine Phasenverschiebungsverschlüsselung (PSK) durchführt.

7. Modulator nach irgendeinem der vorhergehenden Ansprüche, mit einer Datenspeichereinrichtung (32), die zwischen der Transformiereinrichtung (3, 31) und der zweiten Modulationseinrichtung (6, 14b) vorgesehen ist, um zeitweilig die Zeichendaten zu speichern, die in dem dritten digitalen Signal enthalten sind, und um die Zeichendaten, die in der Datenspeichereinrichtung (32) gespeichert sind, der zweiten Modulationseinrichtung (6, 14b) zuzuführen.

8. Modulator nach Anspruch 7, mit einer ein Start- und ein Stoppbit einfügenden Einrichtung (33), die zwischen der Datenspeichereinrichtung (32) und der zweiten Modulationseinrichtung (6, 14b) vorgesehen ist, um jedes Zeichendatum von der Datenspeichereinrichtung (32) zu empfangen und um ein Startbit vor jedes Zeichendatum, welches von der Datenspeichereinrichtung (32) zugeführt wird, und ein Stoppbit nach jedem Zeichendatum einzufügen und um die Zeichendaten mit dem Start- und Stoppbit an die zweite Modulationseinrichtung (6, 14b) zuzuführen.

9. Demodulator, mit:

einer ersten Demodulationseinrichtung (1, 20a, 22a) zum Empfangen eines durch Frequenzteilung gemultiplexten Signals und zum Regenerieren eines ersten digitalen Signals, wobei das erste und das zweite modulierte Signal durch Frequenzteilung in dem durch Frequenzteilung gemultiplexten Signal gemultiplext sind und wobei die Frequenzkomponenten, die in dem ersten modulierten Signal enthalten sind, innerhalb eines ersten Frequenzbandes liegen und die Frequenzkomponenten, die in dem zweiten modulierten Signal enthalten sind, innerhalb eines zweiten Frequenzbandes liegen, welches von dem ersten Frequenzband getrennt ist, wobei das erste modulierte Signal äquivalent einem Signal ist, welches durch die Modulation des ersten digitalen Signals erzeugt wurde, und wobei das zweite modulierte Signal äquivalent einem Signal ist, welches durch Modulieren eines zweiten digitalen Signals erzeugt wurde; und

einer zweiten Demodulationseinrichtung (6, 20b, 22b) zum Empfangen des durch Frequenzteilung gemultiplexten Signals und zum Erzeugen des zweiten digitalen Signals, welches wenigstens einen Satz einer vorbestimmten Anzahl von aufeinanderfolgenden Bits enthält, die Zeichendaten entsprechen; **gekennzeichnet** durch:

eine Transformiereinrichtung (3, 34) zum Empfangen des zweiten digitalen Signals und zum Einfügen eines Startbits vor jedem Satz der vorbestimmten Anzahl von aufeinanderfolgenden Bits, und Einfügen eines Stoppbits nach jedem Satz der vorbestimmten Anzahl von aufeinanderfolgenden Bits, um ein drittes digitales Signal in einem Start-Stopp-System zu erzeugen.

10. Demodulator nach Anspruch 9, bei dem die erste Demodulationseinrichtung (1, 20a, 22a) folgendes aufweist:

eine erste Frequenzschiebeeinrichtung (20a) zum Empfangen des durch Frequenzteilung gemultiplexten Signals und zum Verschieben der Frequenzen des durch Frequenzteilung gemultiplexten Signals um eine erste vorbestimmte Frequenz um das durch Frequenzteilung gemultiplexte Signal in ein viertes digitales Signal zu transformieren, wobei die erste vorbestimmte Frequenz einer Mittenfrequenz des ersten Frequenzbandes entspricht; und

eine erste Bandtrennfiltereinrichtung (22a) zum Empfangen des vierten digitalen Signals und zum Extrahieren des ersten digitalen Signals; und bei dem

die zweite Demodulationseinrichtung (6, 20b, 22b) folgendes enthält:

eine zweite Frequenzschiebeeinrichtung (20a) zum Empfangen des durch Frequenzteilung gemultiplexten Signals und zum Verschieben der Frequenzen des durch Frequenzteilung gemultiplexten Signals um eine zweite vorbestimmte Frequenz, um das durch Frequenzteilung gemultiplexte Signal in ein fünftes digitales Signals zu transformieren, wobei die zweite vorbestimmte Frequenz einer Mittenfrequenz des zweiten Frequenzbandes entspricht; und

eine zweite Bandtrennfiltereinrichtung (22b) zum Empfangen des fünften digitalen Signals und zum Extrahieren des zweiten digitalen Signals.

11. Demodulator nach Anspruch 9 oder 10, mit einer Informationsdecodiereinrichtung (7) zum Empfangen eines digitalen Signals in dem Start-Stopp-System und zum Decodieren der Informationen, die durch das digitale Signal mitgeführt werden.

12. Demodulator nach Anspruch 9, 10 oder 11, bei dem das erste und das zweite modulierte Signal durch den gleichen Modulationstyp moduliert werden und bei dem die erste und die zweite Demodulationseinrichtung wenigstens einen Digitalsignalprozessor aufweisen.

13. Demodulator nach Anspruch 12, bei dem das erste und das zweite modulierte Signal durch eine der Modulationsoperationen, wie Phasenverschiebungsverschlüsselung (PSK) und Quadratamplitudenmodulation (QAM), moduliert werden.

14. Demodulator nach Anspruch 9, 10 oder 11, bei dem wenigstens ein Abschnitt der Operation, die durch die zweite Demodulationseinrichtung durchgeführt wird, ähnlich zu wenigstens einem Abschnitt der Operation ist, die durch die erste Demodulationseinrichtung durchgeführt wird, und bei dem die erste und die zweite Demodulationseinrichtung wenigstens einen Digitalsignalprozessor aufweisen.

15. Demodulator nach Anspruch 14, bei dem die Demodulationsoperation, die durch die erste Demodulationseinrichtung durchführt wird, in Einklang mit der Quadratamplitudenmodulation (QAM) ausgeführt wird und bei dem die Demodulationsoperationen, die durch die zweite Demodulationseinrichtung ausgeführt wird, in Einklang mit der Phasenverschiebungsverschlüsselung (PSK) durchgeführt wird.

16. Demodulator nach irgendeinem der Ansprüche 9 bis 15, mit einer Datenspeichereinrichtung (35), die zwischen der zweiten Demodulationseinrichtung (6, 20b, 22b) und der Transformiereinrichtung (3, 34) vorgesehen ist, um zeitweilig die Zeichendaten zu speichern, die in dem zweiten digitalen Signal enthalten sind, und um die Zeichendaten, die in der Datenspeichereinrichtung (35) gespeichert sind, der Transformiereinrichtung (3, 34) zuzuführen.

17. Demodulator nach Anspruch 16, bei dem das zweite digitale Signal ferner ein Startbit enthält, welches jeden Zeichendaten vorangeht und ein Stoppbit enthält, welches jeden Zeichendaten nachfolgt, und der Demodulator eine Start- und Stoppbit-Entfernungseinrichtung (36) enthält, die zwischen der zweiten Demodulationseinrichtung (6, 20b, 22b) und der Datenspeichereinrichtung (35) vorgesehen ist, um das vierte digitale Signal von der zweiten Demodulationseinrichtung (6, 20b, 22b) zu empfangen, ein Startbit zu entfernen, welches jeden Zeichendaten vorangeht und ein Stoppbit zu entfernen, welches jeden Zeichendaten nachfolgt und um die Zeichendaten ohne die Start- und Stoppbits der Datenspeichereinrichtung (35) zuzuführen.

18. Modem mit einem Modulator nach irgendeinem der Ansprüche 1 bis 8 und mit einem Demodulator nach irgendeinem der Ansprüche 9 bis 17.

Revendications

1. Modulateur comprenant :

un premier moyen de modulation (1, 14a) pour recevoir un premier signal numérique et pour moduler le premier signal numérique afin de générer un premier signal modulé, où des composantes de fréquence contenues dans le premier signal modulé sont dans une première bande de fréquences ;
un second moyen de modulation (6, 14b) pour recevoir un autre signal numérique et pour le moduler afin de générer un second signal modulé, où des composantes de fréquence contenues dans le second signal modulé sont dans une seconde bande de fréquences qui est séparée de la première bande de fréquences ; et un moyen d'addition de signal (4, 15) pour recevoir les premier et second signaux modulés et pour additionner les premier et second signaux modulés afin de générer un signal multiplexé par division en fréquence,

caractérisé par :
un moyen de transformation (3, 31) pour recevoir un second signal numérique contenant au moins un jeu d'un nombre prédéterminé de bits successifs correspondant à des données de caractère, un bit de départ précédant chaque jeu du nombre prédéterminé de bits successifs et un bit d'arrêt suivant chaque jeu du nombre prédéterminé de bits successifs, et pour enlever le bit de départ et le bit d'arrêt du second signal numérique afin de générer un troisième signal numérique contenant les données de caractère en tant que dit autre signal numérique reçu par ledit second moyen de modulation (6, 14b).

2. Modulateur selon la revendication 1, comprenant en outre un moyen de génération de signal numé-

rique (7) pour générer le second signal numérique afin d'appliquer le second signal numérique sur le moyen de transformation (3, 31).

3. Modulateur selon la revendication 1 ou 2, dans lequel les premier et second moyens de modulation réalisent le même type de modulation et les premier et second moyens de modulation comprennent au moins un processeur de signal numérique.

4. Modulateur selon la revendication 3, dans lequel les premier et second moyens de modulation réalisent une modulation par décalage de phase (PSK) ou une modulation d'amplitude en quadrature (QAM).

5. Modulateur selon la revendication 1 ou 2, dans lequel au moins une partie de l'opération réalisée par le second moyen de modulation est similaire à au moins une partie de l'opération réalisée par le premier moyen de modulation, et les premier et second moyens de modulation comprennent au moins un processeur de signal numérique.

6. Modulateur selon la revendication 5, dans lequel le premier moyen de modulation réalise une modulation d'amplitude en quadrature (QAM) et le second moyen de modulation réalise une modulation par décalage de phase (PSK).

7. Modulateur selon l'une quelconque des revendications précédentes, comprenant un moyen de stockage de données (32), prévu entre le moyen de transformation (3, 31) et le second moyen de modulation (6, 14b), pour stocker temporairement les données de caractère contenues dans le troisième signal numérique et pour appliquer les données de caractère stockées dans le moyen de stockage de données (32) sur le second moyen de modulation (6, 14b).

8. Modulateur selon la revendication 7, comprenant un moyen d'insertion de bits de départ et d'arrêt (33), prévu entre le moyen de stockage de données (32) et le second moyen de modulation (6, 14b), pour recevoir chaque donnée de caractère depuis le moyen de stockage de données (32), pour insérer un bit de départ avant chaque donnée de caractère appliquée depuis le moyen de stockage de données (32) et un bit d'arrêt après chaque donnée de caractère et pour appliquer les données de caractère avec les bits de départ et d'arrêt sur le second moyen de modulation (6, 14b).

9. Démodulateur comprenant :

un premier moyen de démodulation (1, 20a, 22a) pour recevoir un signal multiplexé par division en fréquence et pour régénérer un premier signal numérique, dans lequel des premier et second signaux modulés sont multiplexés par division en fréquence dans le signal multiplexé par division en fréquence et dans lequel des composantes de fréquence contenues dans le premier signal modulé sont dans une première bande de fréquences et des composantes de fréquence contenues dans le second signal modulé sont dans une seconde bande de fréquences qui est séparée de la première bande de fréquences, le premier signal modulé étant équivalent à un signal généré en modulant le premier signal numérique et le second signal modulé étant équivalent à un signal généré en modulant un second signal numérique ; et

un second moyen de démodulation (6, 20b, 22b) pour recevoir le signal multiplexé par division en fréquence et pour régénérer le second signal numérique contenant au moins un jeu d'un nombre prédéterminé de bits successifs correspondant à des données de caractère,

caractérisé par :

un moyen de transformation (3, 34) pour recevoir le second signal numérique et pour insérer un bit de départ avant chaque jeu du nombre prédéterminé de bits successifs et un bit d'arrêt après chaque jeu du nombre prédéterminé de bits successifs afin de générer un troisième signal numérique dans un système à départ-arrêt.

10. Démodulateur selon la revendication 9, dans lequel ledit premier moyen de démodulation (1, 20a, 22a) comprend :

un premier moyen de décalage en fréquence (20a) pour recevoir le signal multiplexé par division en fréquence et pour décaler des fréquences du signal multiplexé par division en fréquence d'une première fréquence prédéterminée afin de transformer le signal multiplexé par division en fréquence selon un quatrième signal numérique, où la première fréquence prédéterminée correspond à une fréquence centrale de la première bande de fréquences ; et

un premier moyen de filtre de séparation de bande (22a) pour recevoir le quatrième signal numérique et pour extraire le premier signal numérique ; et

dans lequel :

le second moyen de démodulation (6, 20b, 22b) comprend :

un second moyen de décalage en fréquence (20a) pour recevoir le signal multiplexé par di-

vision en fréquence et pour décaler les fréquences du signal multiplexé par division en fréquence d'une seconde fréquence prédéterminée afin de transformer le signal multiplexé par division en fréquence selon un cinquième signal numérique, où la seconde fréquence prédéterminée correspond à une fréquence centrale de la seconde bande de fréquences ; et

un second moyen de filtre de séparation de bande (22b) pour recevoir le cinquième signal numérique et pour extraire le second signal numérique.

11. Démodulateur selon la revendication 9 ou 10, comprenant un moyen de décodage d'information (7) pour recevoir un signal numérique dans le système à départ-arrêt et pour décoder une information transportée par le signal numérique.

12. Démodulateur selon la revendication 9, 10 ou 11, dans lequel les premier et second signaux modulés sont modulés au moyen du même type de modulation et les premier et second moyens de démodulation comprennent au moins un processeur de signal numérique.

13. Démodulateur selon la revendication 12, dans lequel les premier et second signaux modulés sont modulés au moyen d'une modulation par décalage de phase (PSK) ou d'une modulation d'amplitude en quadrature (QAM).

14. Démodulateur selon la revendication 9, 10 ou 11, dans lequel au moins une partie de l'opération réalisée par le second moyen de démodulation est similaire à au moins une partie de l'opération réalisée par le premier moyen de démodulation, et les premier et second moyens de démodulation comprennent au moins un processeur de signal numérique.

15. Démodulateur selon la revendication 14, dans lequel l'opération de démodulation réalisée par le premier moyen de démodulation est conforme à une modulation d'amplitude en quadrature (QAM) et l'opération de démodulation réalisée par le second moyen de démodulation est conforme à une modulation par décalage de phase (PSK).

16. Démodulateur selon l'une quelconque des revendications 9 à 15, comprenant un moyen de stockage de données (35), prévu entre le second moyen de démodulation (6, 20b, 22b) et le moyen de transformation (3, 34), pour stocker temporairement les données de caractère contenues dans le second signal numérique et pour appliquer les données de caractère stockées dans le moyen de stockage de données (35) sur le moyen de transformation (3, 34).

17. Démodulateur selon la revendication 16, dans lequel le second signal numérique contient en outre un bit de départ qui précède chaque donnée de caractère et un bit d'arrêt qui suit chaque donnée de caractère; et

ledit démodulateur comprend un moyen d'enlèvement de bits de départ et d'arrêt (36), prévu entre le second moyen de démodulation (6, 20b, 22b) et le moyen de stockage de données (35), pour recevoir le quatrième signal numérique depuis le second moyen de démodulation (6, 20b, 22b), pour enlever un bit de départ qui précède chaque donnée de caractère et un bit d'arrêt qui suit chaque donnée de caractère et pour appliquer les données de caractère sans les bits de départ et d'arrêt sur le moyen de stockage de données (35).

18. Modem comprenant un modulateur selon l'une quelconque des revendications 1 à 8 et un démodulateur selon l'une quelconque des revendications 9 à 17.

Fig. 1

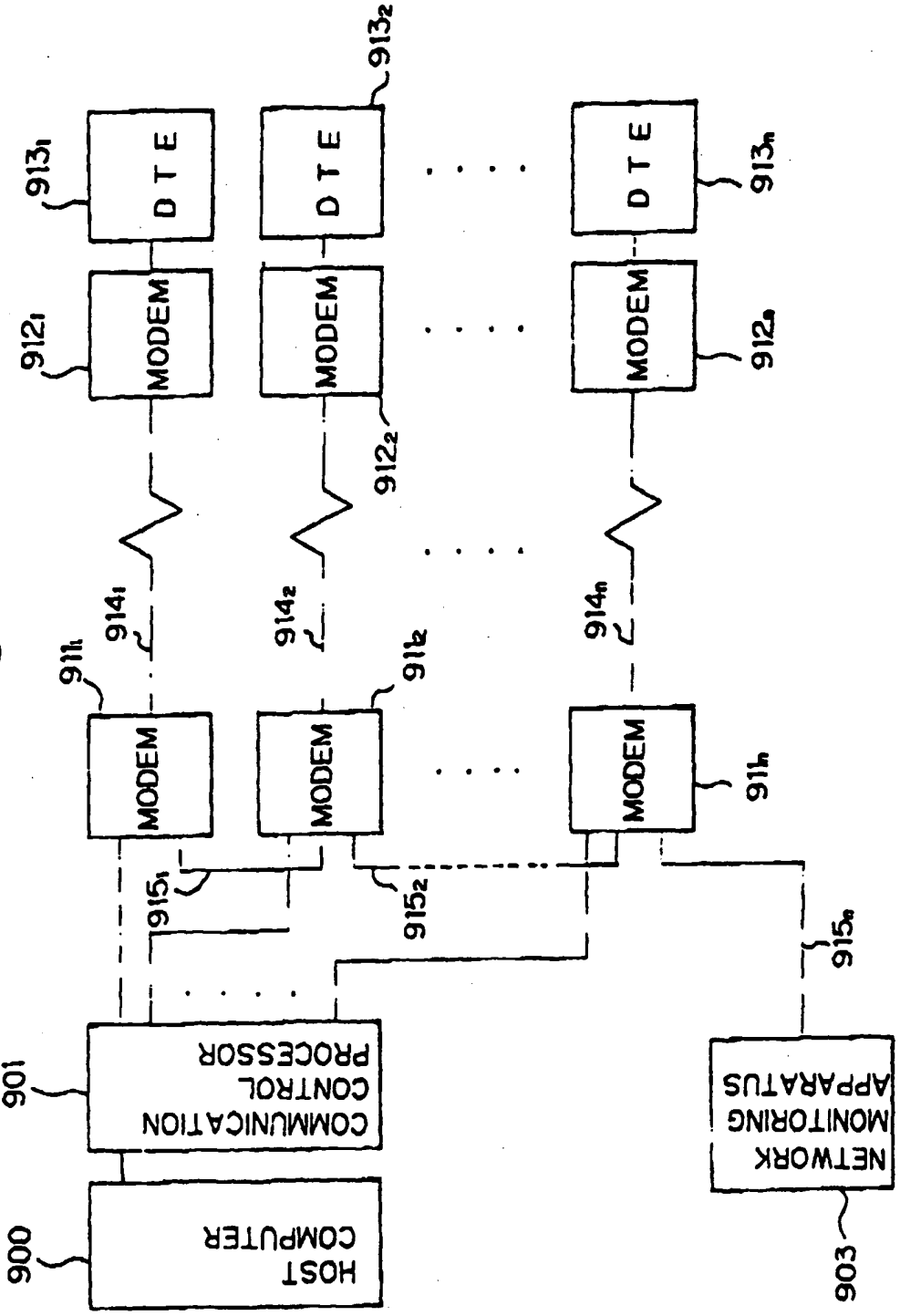

HOST COMPUTER
900
COMMUNICATION CONTROL PROCESSOR
901
NETWORK MONITORING APPARATUS
903
MODEM
911₁
MODEM
911₂
MODEM
911ₙ
MODEM
912₁
MODEM
912₂
MODEM
912ₙ
DTE
913₁
DTE
913₂
DTE
913ₙ
914₁
914₂
914ₙ
915₁
915₂
915ₙ

Fig. 2

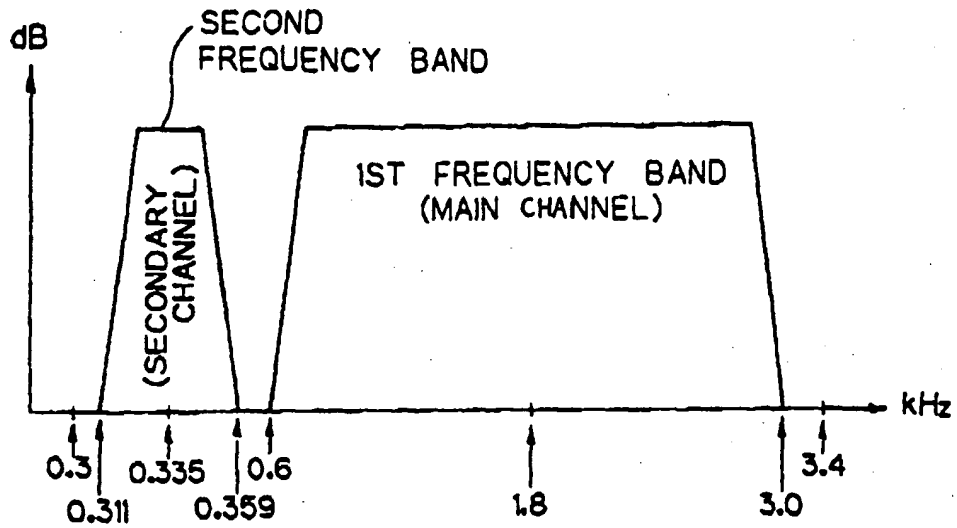

dB
SECOND
FREQUENCY BAND
(SECONDARY CHANNEL)
1ST FREQUENCY BAND
(MAIN CHANNEL)
kHz
0.3
0.311
0.335
0.359
0.6
1.8
3.0
3.4

Fig. 3

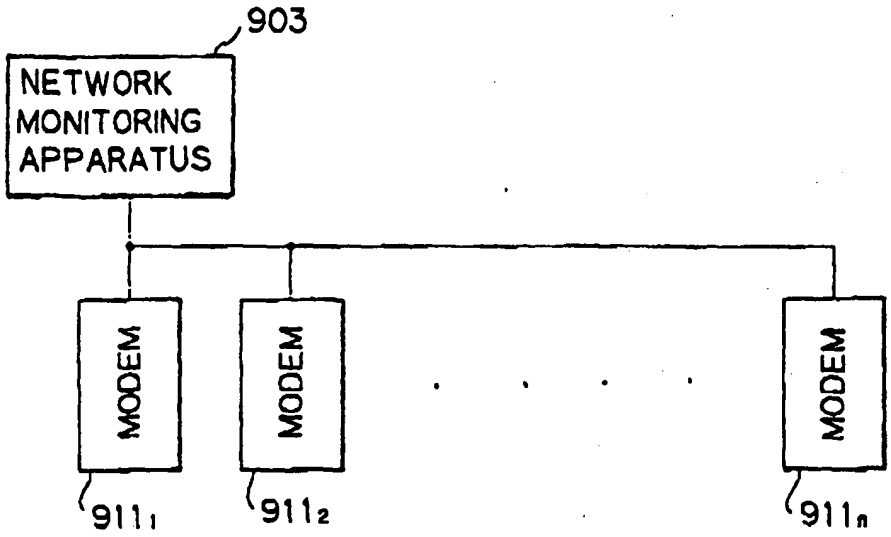
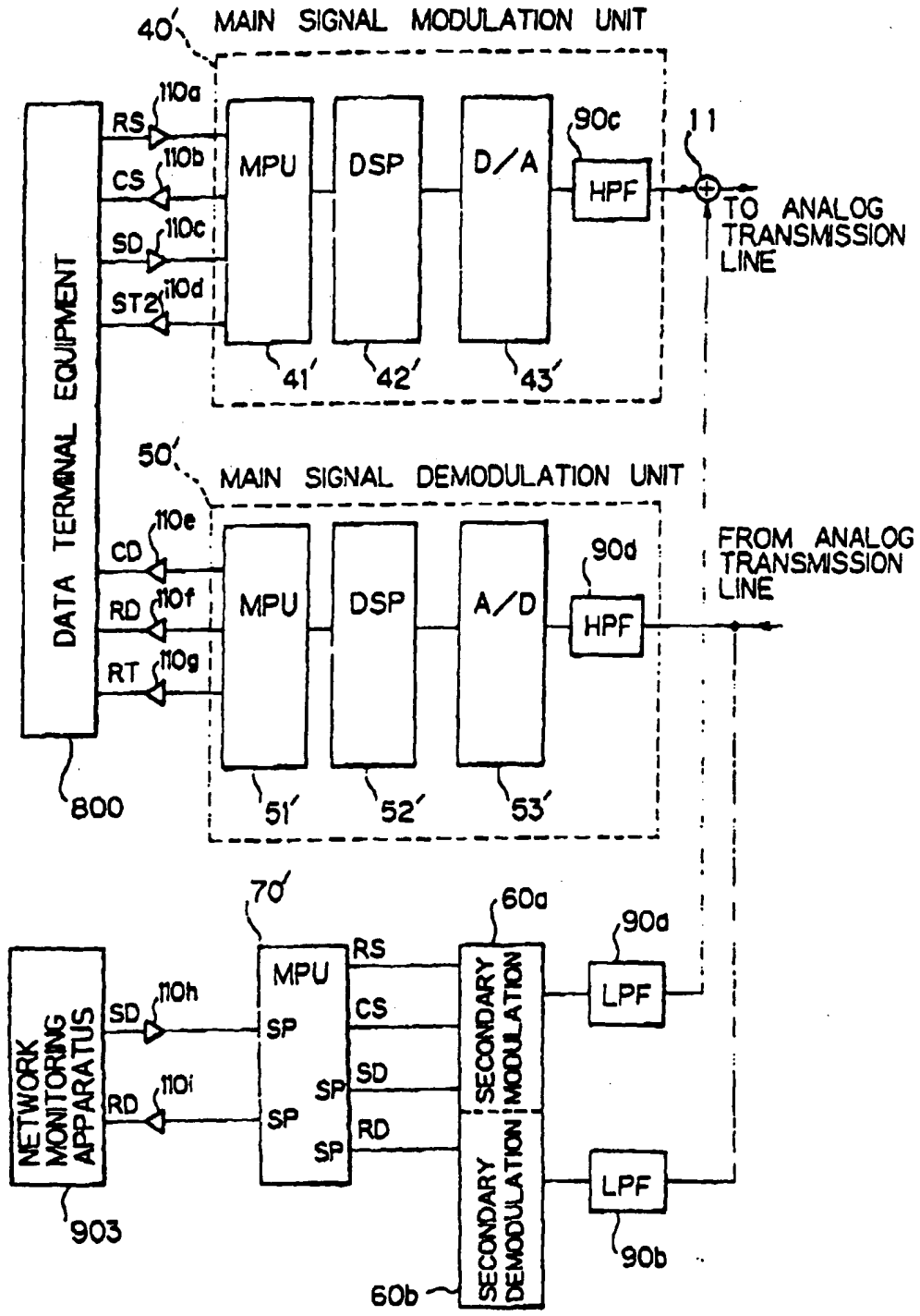

903
NETWORK
MONITORING
APPARATUS
MODEM
MODEM
MODEM
911₁
911₂
911n

Fig. 4


40'
MAIN SIGNAL MODULATION UNIT
110a
RS
110b
CS
110c
SD
110d
ST2
MPU
DSP
D/A
90c
HPF
11
TO ANALOG TRANSMISSION LINE
41'
42'
43'
DATA TERMINAL EQUIPMENT
50'
MAIN SIGNAL DEMODULATION UNIT
110e
CD
110f
RD
110g
RT
MPU
DSP
A/D
90d
HPF
FROM ANALOG TRANSMISSION LINE
51'
52'
53'
800
70'
60a
90a
NETWORK MONITORING APPARATUS
110h
SD
110i
RD
MPU
SP
SP
SP
SP
RS
CS
SD
RD
SECONDARY MODULATION
SECONDARY DEMODULATION
LPF
LPF
903
60b
90b

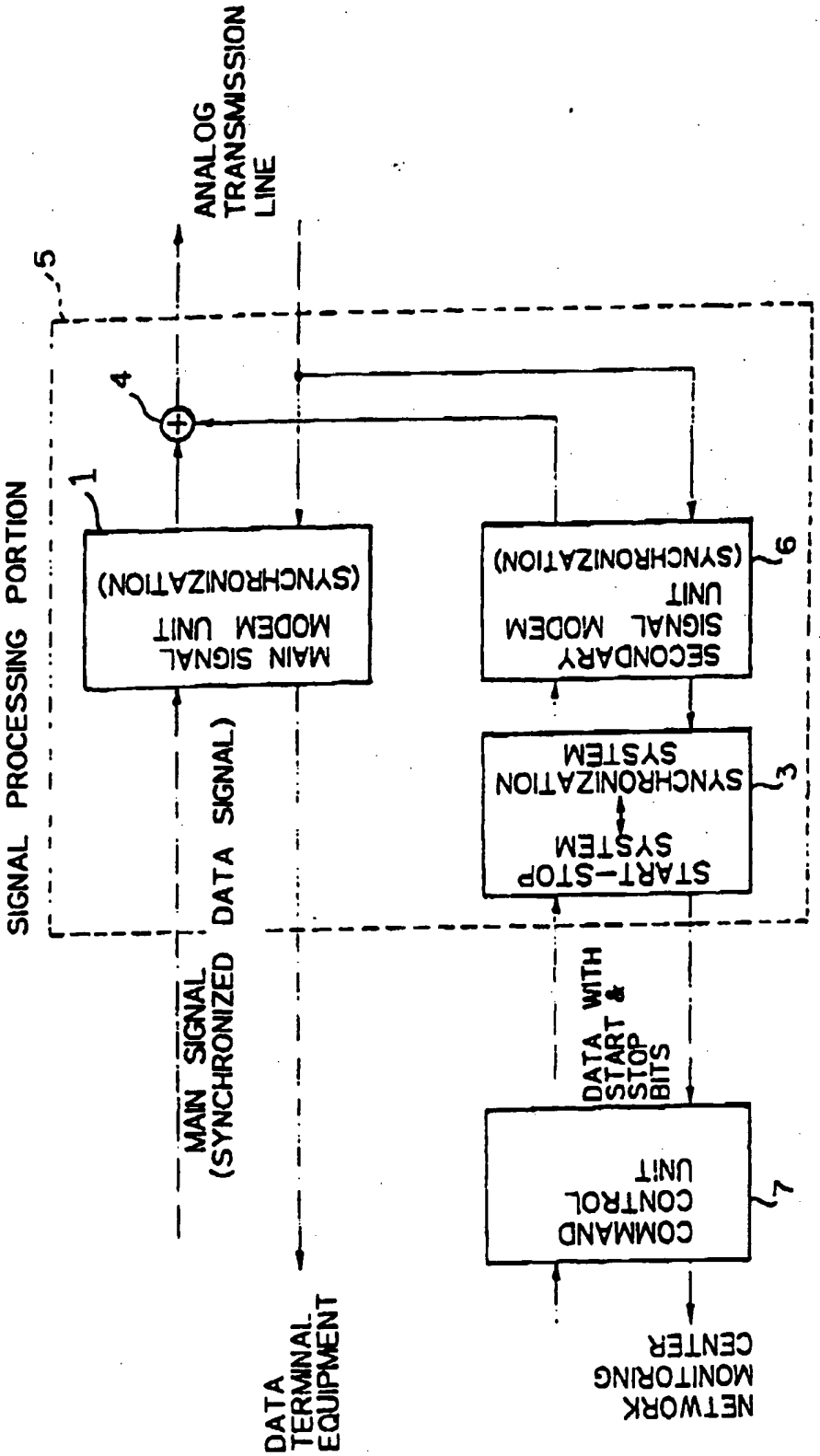

ANALOG TRANSMISSION LINE
5
SIGNAL PROCESSING PORTION
4
1
MAIN SIGNAL MODEM UNIT (SYNCHRONIZATION)
SECONDARY SIGNAL MODEM UNIT (SYNCHRONIZATION)
6
SYNCHRONIZATION SYSTEM
3
START-STOP SYSTEM
MAIN SIGNAL (SYNCHRONIZED DATA SIGNAL)
DATA WITH START & STOP BITS
COMMAND CONTROL UNIT
7
DATA TERMINAL EQUIPMENT
NETWORK MONITORING CENTER

Fig. 5

Fig. 6

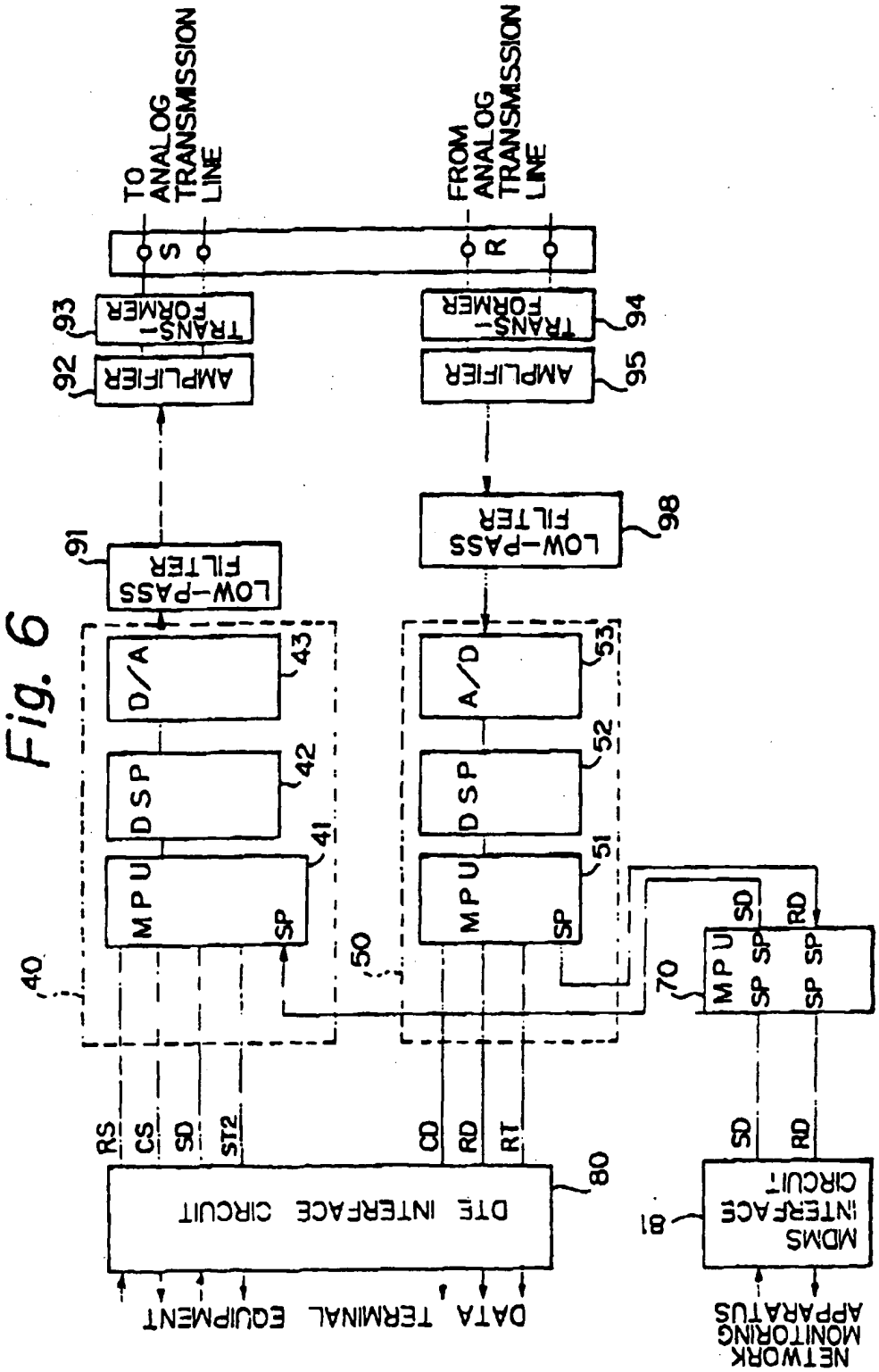

TO ANALOG TRANSMISSION LINE
FROM ANALOG TRANSMISSION LINE
S
R
TRANS-FORMER
93
94
AMPLIFIER
92
95
LOW-PASS FILTER
91
98
D/A
43
A/D
53
DSP
42
52
MPU
41
51
SP
40
50
70
SD
RD
RS
CS
SD
ST2
CD
RD
RT
80
DTE INTERFACE CIRCUIT
81
MDMS INTERFACE CIRCUIT
DATA TERMINAL EQUIPMENT
NETWORK MONITORING APPARATUS

Fig. 7

Fig. 7A | Fig. 7B

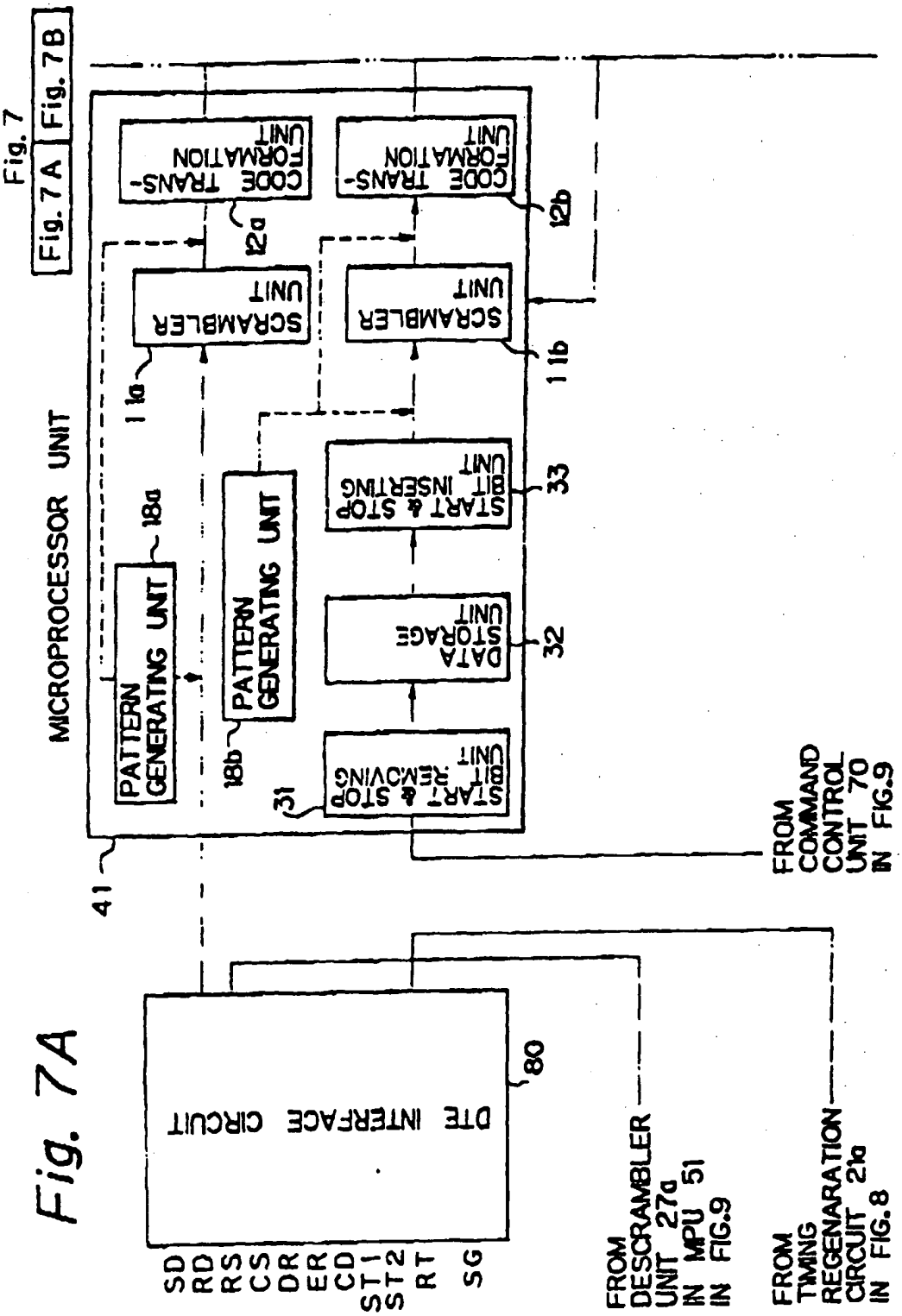


Fig. 7A

Fig. 7B

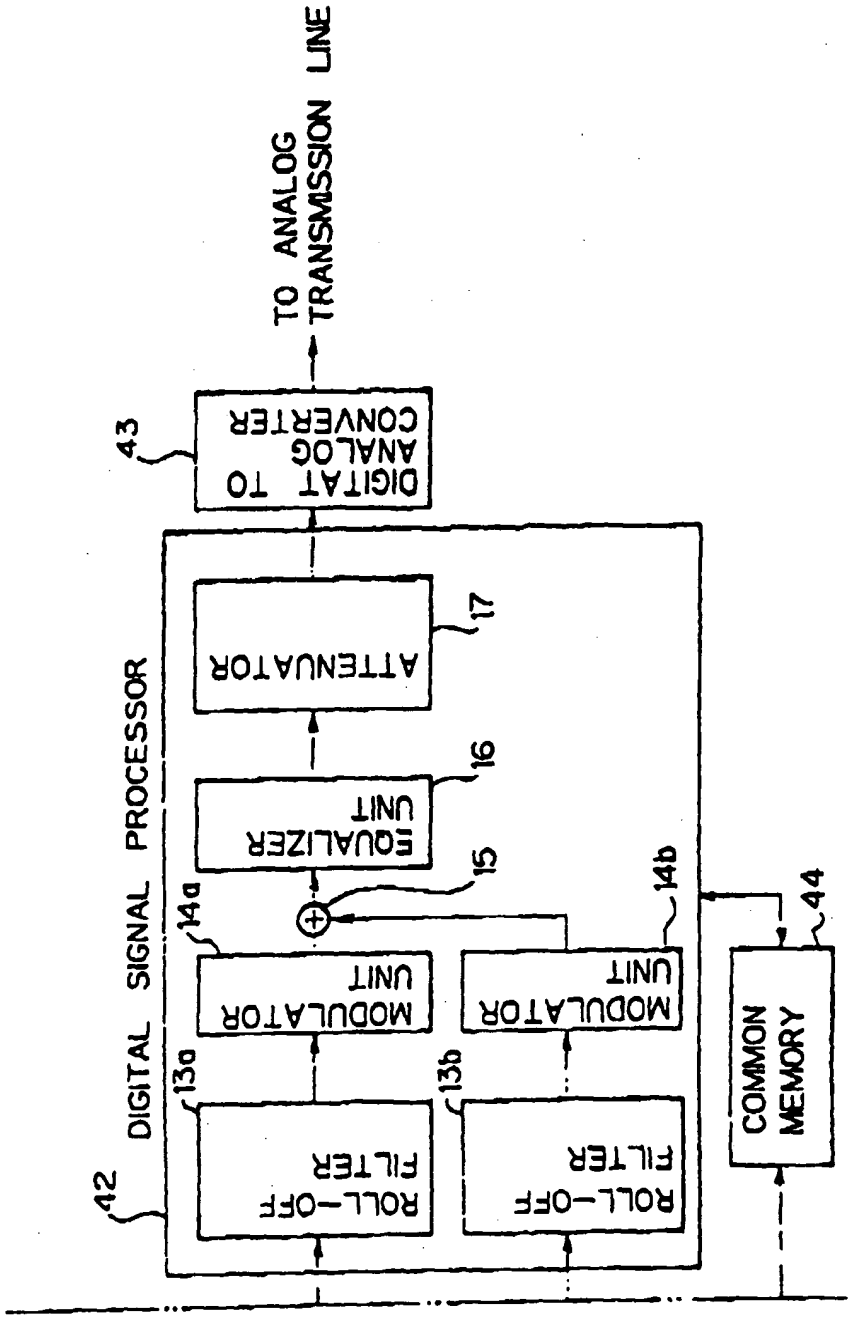

TO ANALOG TRANSMISSION LINE
43
DIGITAT TO ANALOG CONVERTER
DIGITAL SIGNAL PROCESSOR
42
ATTENUATOR
17
EQUALIZER UNIT
16
15
14a
14b
MODULATOR UNIT
MODULATOR UNIT
13a
13b
ROLL-OFF FILTER
ROLL-OFF FILTER
COMMON MEMORY
44

Fig. 8A

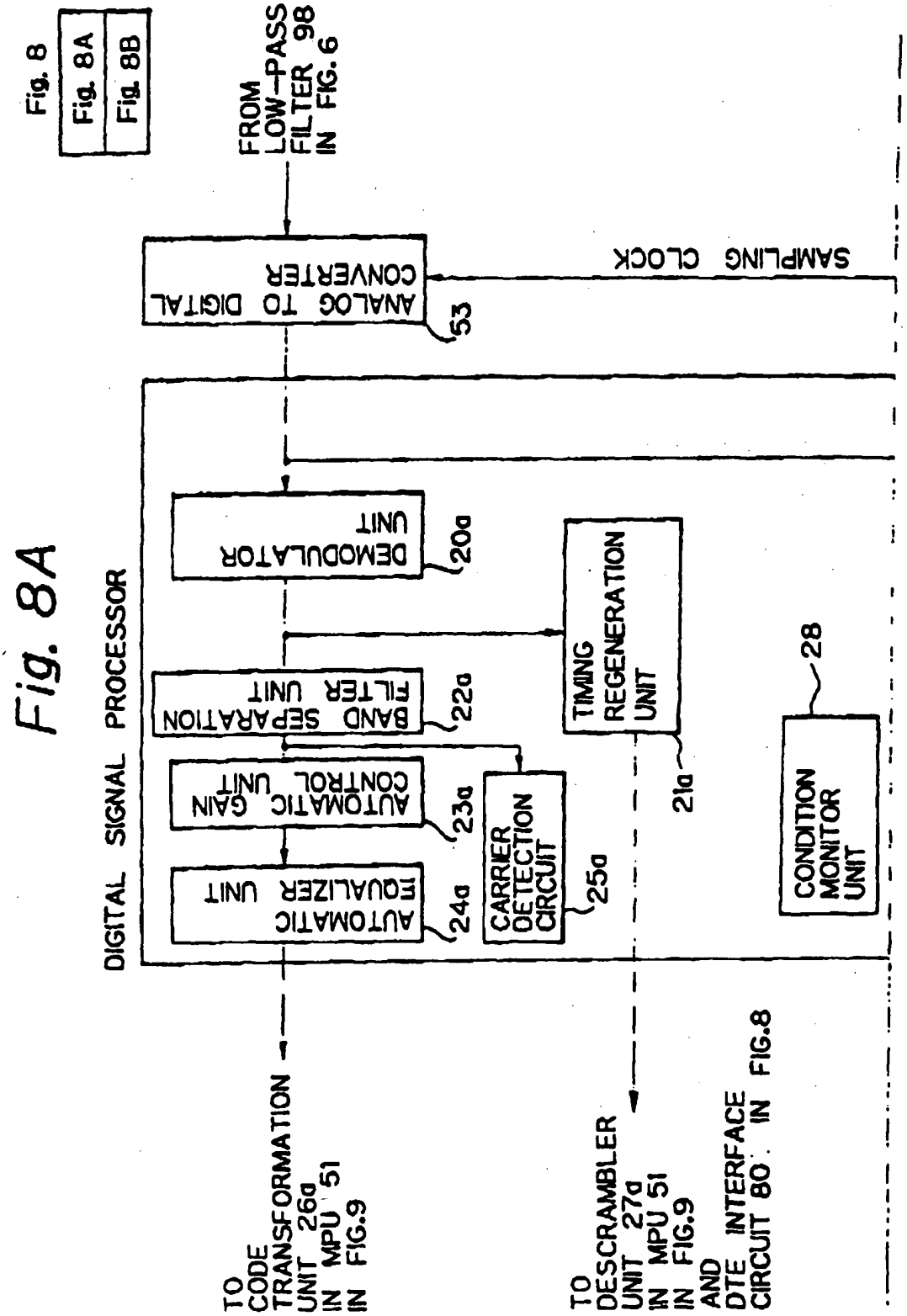


Fig. 8
Fig. 8A
Fig. 8B
FROM LOW-PASS FILTER 98 IN FIG. 6
ANALOG TO DIGITAL CONVERTER
53
SAMPLING CLOCK
DIGITAL SIGNAL PROCESSOR
DEMODULATOR UNIT
20a
BAND SEPARATION FILTER UNIT
22a
AUTOMATIC GAIN CONTROL UNIT
23a
AUTOMATIC EQUALIZER UNIT
24a
CARRIER DETECTION CIRCUIT
25a
TIMING REGENERATION UNIT
21a
28
CONDITION MONITOR UNIT
TO CODE TRANSFORMATION UNIT 26a IN MPU 51 IN FIG.9
TO DESCRAMBLER UNIT 27a IN MPU 51 IN FIG.9 AND DTE INTERFACE CIRCUIT 80 IN FIG.8

Fig. 8B

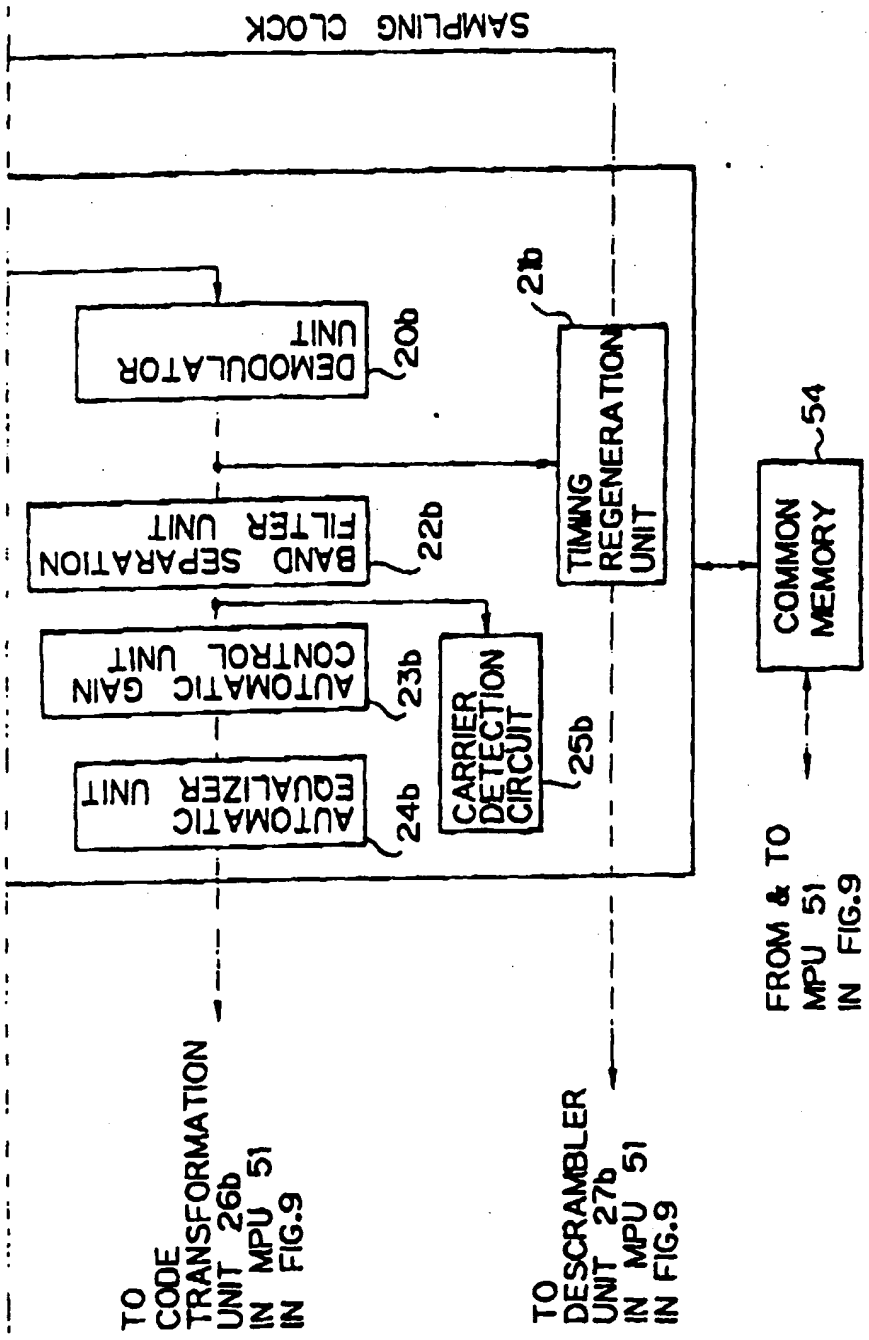

SAMPLING CLOCK
DEMODULATOR UNIT
20b
21b
TIMING REGENERATION UNIT
54
COMMON MEMORY
BAND SEPARATION FILTER UNIT
22b
AUTOMATIC GAIN CONTROL UNIT
23b
CARRIER DETECTION CIRCUIT
25b
AUTOMATIC EQUALIZER UNIT
24b
TO CODE TRANSFORMATION UNIT 26b IN MPU 51 IN FIG.9
TO DESCRAMBLER UNIT 27b IN MPU 51 IN FIG.9
FROM & TO MPU 51 IN FIG.9

Fig. 9

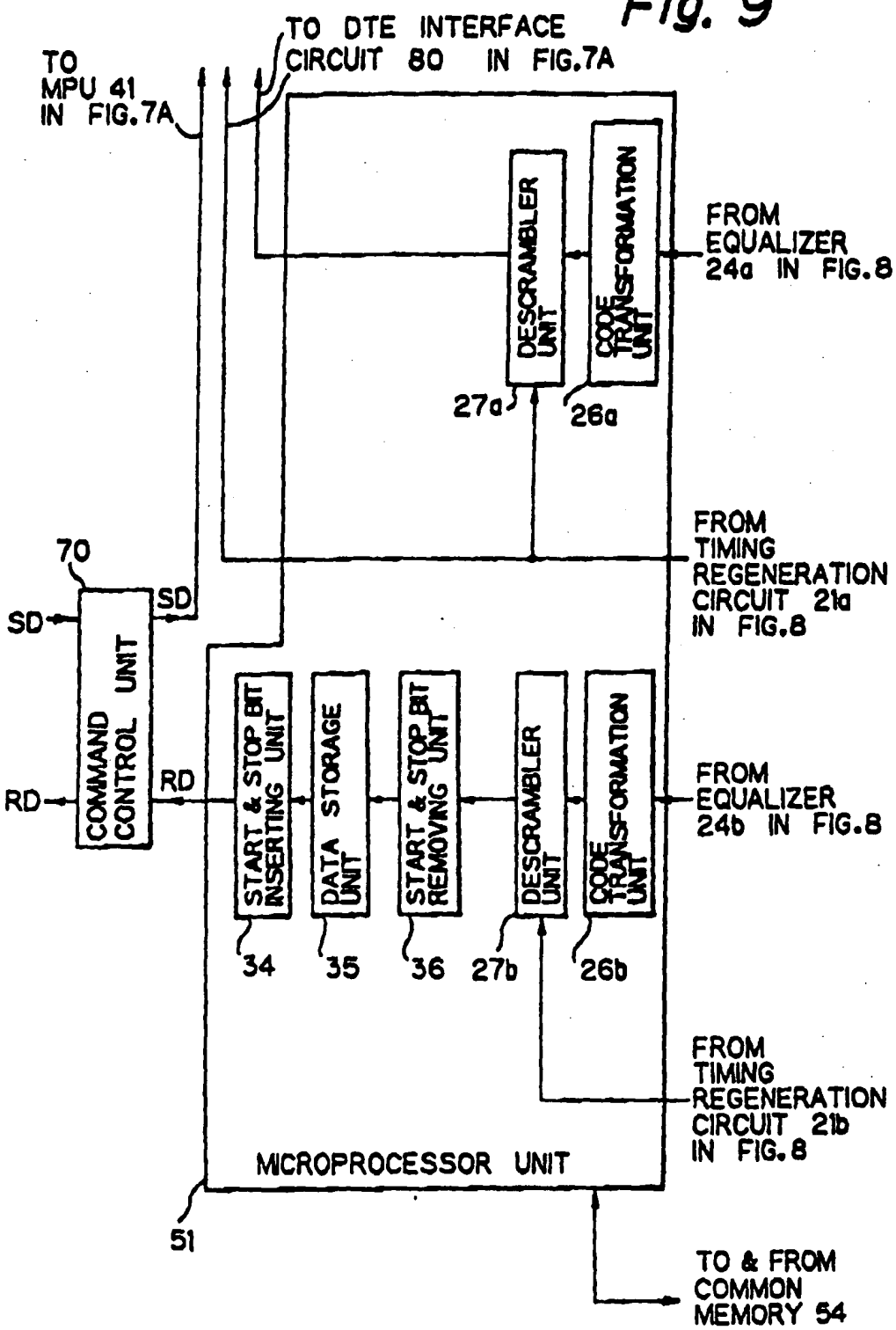

TO DTE INTERFACE CIRCUIT 80 IN FIG.7A
TO MPU 41 IN FIG.7A
DESCRAMBLER UNIT
CODE TRANSFORMATION UNIT
FROM EQUALIZER 24a IN FIG.8
27a
26a
FROM TIMING REGENERATION CIRCUIT 21a IN FIG.8
70
SD
SD
COMMAND CONTROL UNIT
RD
RD
START & STOP BIT INSERTING UNIT
DATA STORAGE UNIT
START & STOP BIT REMOVING UNIT
DESCRAMBLER UNIT
CODE TRANSFORMATION UNIT
FROM EQUALIZER 24b IN FIG.8
34
35
36
27b
26b
FROM TIMING REGENERATION CIRCUIT 21b IN FIG.8
MICROPROCESSOR UNIT
51
TO & FROM COMMON MEMORY 54

Fig. 10

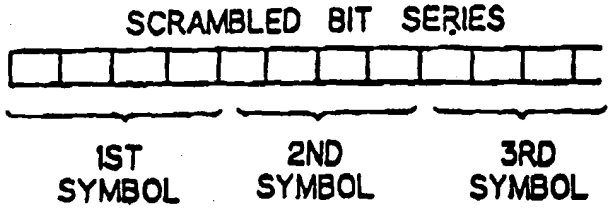


Fig. 11

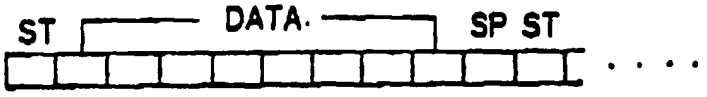
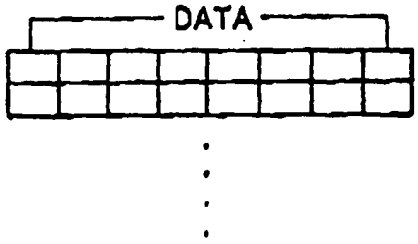



Fig. 12